AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

Claim 1 (currently amended) A method of manufacturing an electronic parts packaging structure, comprising the steps of:

flip-chip connecting a connection terminal of an electronic parts having the connection terminal on an element forming surface to a wiring pattern formed on or over a base substrate;

forming an insulating film in which the electronic parts are buried, on the electronic parts and the wiring substrate ~~for covering the electronic parts~~;

forming a via hole having a depth that reaches the connection terminal by etching a predetermined portion from an upper surface of the insulating film to the element forming surface of the electronic parts; and

forming an overlying wiring pattern, which is connected to the connection terminal via the via hole, on the insulating film.

Claim 2 (currently amended) A method of manufacturing an electronic parts packaging structure, comprising the steps of:

flip-chip connecting a connection terminal of an electronic parts, which has the

connection terminal on an element forming surface and has a through electrode connected to the connection terminal via a first via hole on a back surface, to a wiring pattern formed on or over a wiring substrate;

forming an insulating film in which the electronic parts are buried, on the electronic parts and the wiring substrate ~~for covering the electronic parts~~;

forming a second via hole having a depth that reaches the through electrode, by etching a predetermined portion of the insulating film on the through electrode; and

forming an overlying wiring pattern, which is connected to the through electrode via the second via hole, on the insulating film.

Claim 3 (original) A method of manufacturing an electronic parts packaging structure, according to claim 1, wherein, in the step of forming the via hole, the insulating film and the electronic parts are etched by RIE or a laser.

Claim 4 (currently amended) A method of manufacturing an electronic parts packaging structure, according to claim 1, wherein the step of forming the overlying wiring pattern includes the steps of[[,]]:

forming a resist film having an opening portion in a predetermined portion containing the via hole on the insulating film[[,]];

forming a conductive film pattern in the via hole and the opening portion of the resist

film, by applying a plating upward from the connection terminal exposed from a bottom portion of the via hole by means of electroplating that utilizes the wiring pattern and the connection terminal of the electronic parts connected to the wiring pattern as a plating power-supply layer[[,]]; and

removing the resist film to get the overlying wiring pattern.

Claim 5 (original) A method of manufacturing an electronic parts packaging structure, according to claim 1, after the step of forming the via hole but before the step of forming the overlying wiring pattern, further comprising the steps of:

forming an inorganic insulating film on an inner surface of the via hole and on the insulating film; and

removing the inorganic insulating film from a bottom portion of the via hole to expose the connection terminal on the bottom portion of the via hole.

Claim 6 (original) A method of manufacturing an electronic parts packaging structure, according to claim 1, wherein a structure in which a plurality of electronic parts are stacked three-dimensionally in a multi-layered fashion and are connected mutually via the via hole is formed by repeating n times (n is an integer of 1 or more) respective steps from the step of flip-chip connecting the electronic parts to the wiring pattern to the step of forming the overlying wiring pattern.

Claim 7 (original) A method of manufacturing an electronic parts packaging structure, according to claim 1, after the step of forming the overlying wiring pattern, further comprising the step of:

flip-chip connecting a connection terminal of an overlying electronic parts having the connection terminal to the overlying wiring pattern.

Claim 8 (original) A method of manufacturing an electronic parts packaging structure, according to claim 1, wherein the electronic parts is a semiconductor chip whose thickness is about 150 μm or less.